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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,715	06/26/2003	Benjamin Thomas Percer	200312936-1	5780

22879 7590 08/31/2006

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,715	PERCER ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13-24 and 29-32* is/are rejected.

7)☒ Claim(s) *9-12 and 25-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to applicant's response received on 07/19/2006.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 24-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real word" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S.519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993).

A process that consists solely of the manipulation of an abstract idea is not concrete or tangible. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459. Nor can one patent "a novel and useful mathematical formula," Flook, 437 U.S. at 585, 198 USPQ at 195; electromagnetism or

steam power, O'Reilly v. Morse, 56 U.S. (15 How.) 62, 113-114 (1853). To view the new guidelines for 35 U.S.C. 101, please view the following OG notice.

http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm

With respect to claims 24-29, the method of masking fault during margin testing in a computer system. Merely generating signal indicative of absence of faults would appear to be sufficient to constitute a tangible result, since the outcome of the generating signal indicative of absence of faults step has not been used in a disclosed practical application nor made available in such manner that it's usefulness in a disclosed practical application can be relized. It is unclear how the result is being stored, displayed, or used in any tangible manner. In order to overcome the rejection, the claim language should be added that includes displaying, storing, or conveying used in tangible results.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-8, 13, 15-17, 22, 24, 29, and 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Coyle et al. (USP 6,546,507).

Regarding claims 1, 22, 24, and 31, Coyle et al. disclose a system for margin testing one or more components of an electronic system (computer's bus system)(Col.33, lines 8-13, Col.34, lines 7-20), comprising a fault bypass module (a failure capture module 2506) incorporated in said electronic system (bus 2502), said fault bypass module (failure capture module 2506) configured to indicate of one or more faults associated with one or more of said components (bus 2502) during margin testing of said electronic system (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34) and mask the at least one signal indicative of one or more faults (not pass the value) by generating at least one signal indicative of absence of the one or more faults (pass the value) (e.g. Figs.28C, 28D, Col.39, line 42-Col.40, line 12); and an internal controller (a program control module 2512) in communication with said fault bypass module (failure capture module 2506), said internal controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module (e.g. Fig.25, Col.34, lines 62-65, Col.39, line 42-Col.40, line 12).

Regarding claim 32, Coyle et al. disclose a computer server (e.g. Col.31, lines 21-23, 31-35, Col.32, lines 59-62), comprising a margin testing system for margin testing one or more components of the computer server (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34), the margin testing system comprising: a fault bypass module (a failure capture module 2506) incorporated in said computer server (bus 2502 of computer sever); said fault

bypass module configured to mask signals indicative of one or more faults associated with one or more of said components during margin testing of said computer server (e.g. Fig.25, Col.34, lines 62-65, Figs.28C, 28D, Col.39, line 42-Col.40, line 12).

Regarding claim 2, Coyle et al. disclose at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold (e.g. Col.35, lines 50-65).

Regarding claim 3, Coyle et al. disclose said operating parameter is any of voltage (e.g. Col.35, lines 50-65).

Regarding claim 4, Coyle et al. disclose a controller (program control module 2512) incorporated in said electronic system and in communication with said fault bypass module (failure capture module 2506), said controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module (e.g. Fig.25, Col.34, lines 62-65, Col.39, line 42-Col.40, line 12).

Regarding claim 5, Coyle et al. disclose said fault signals comprise one or more interrupt signals (e.g. Col.14, lines 36-48, Col.30 lines 60-63, Col.44, lines 28-32).

Regarding claim 6, Coyle et al. disclose said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system (e.g.Col.9, lines 35-39, Col.37, lines 28-32).

Regarding claim 7, Coyle et al. disclose a hardware monitor (stress injection module 2504) configured to communication with said controller

(program control module 2512) and with at least one of said one or more components (failure capture module 2506), and to generate a fault signal in response to an occurrence of a fault associated with said at least one component (failure capture module 2506) (e.g. Fig.25, Col.35, lines 5-30).

Regarding claim 8, Coyle et al. disclose said hardware monitor (stress injection module 2504) is further configured to transmit said fault signal to said fault bypass module (failure capture module 2506), and wherein said fault bypass module (failure capture module 2506) is further configured to mask said received fault signal during margin testing of said electronic device (e.g. Fig.25, Col.35, lines 5-30, Col.36, lines 23-29).

Regarding claim 13, Coyle et al. disclose a programmable logic device (FFM logic 120) programmed to provide masking of said fault signals (e.g. Col.35, lines 18-26).

Regarding claims 15 and 29, Coyle et al. disclose said fault bypass module(failure capture module 2506) is further configured to intercept a selected output signal of said at least one component and to generate a simulated signal corresponding to said intercepted output signal (e.g. Col.14, lines 36-48, Col.30 lines 60-63, Col.44, lines 28-32) for transmittal to said hardware monitor (stress injection module 2504) during margin testing of said component (e.g. Fig.25, Col.35, lines 5-30, Col.36, lines 23-29).

Regarding claim 16, Coyle et al. disclose said electronic system comprises a computer system (e.g. Col.31, lines 31-35, Col.32, lines 59-62).

Regarding claim 17, Coyle et al. disclose computer system is a computer server (e.g. Col.31, lines 21-23).

Regarding claim 30, Coyle et al. disclose said electronic system is a computer server (e.g. Col.31, lines 21-23, 31-35, Col.32, lines 59-62).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al. (USP 6,546,507) in view of Taraci et al. (USP 5,119,021).

Regarding claim 14, Coyle et al. fail to disclose a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor.

Taraci et al. teach a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor (e.g. Col.6, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a temperature diode coupled to at least one of said components and configured to measure a temperature of said component

and to supply said measured temperature to said hardware monitor as taught by Taraci et al. in a margin test method of Coyle et al. for the purpose of providing a method and apparatus for maintaining a desired case temperature of an electrically operating device undergoing a burn-in test (Taraci et al., Col.3, lines 65-68).

8. Claim 18-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al. (USP 6,546,507) in view of Hawkins et al. (US 2003/0130969 A1).

Regarding claims 18-21 and 23, Coyle et al. fail to disclose a controller comprises a Baseboard Management Controller (BMC), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB).

Hawkins et al. disclose a controller comprises a Baseboard Management Controller (BMC) ([0015]-[0017]), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus)([0006]), wherein said I^2C bus is IPMB ([0013]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Baseboard Management Controller (BMC), an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB) as taught by Hawkins et al. in a margin test method of Coyle et al. for the purpose of providing a star Intelligent Platform Management Bus Topology.

Allowable Subject Matter

9. Claims 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 25-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended to overcome the rejection(s) under 35 U.S.C. 101, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, in combination with other limitations of the claims, none of the prior art of record teaches or suggests the combination of a margin testing system for margin testing one or more components of the computer system, comprising: a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 11, in combination with other limitations of the claims, none of the prior art of record teaches or suggests the combination of a margin testing system for margin testing one or more components of the computer system, comprising: a hardware monitor in communication with said controller

and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component; wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 25, in combination with other limitations of the claims, none of the prior art of record teaches or suggests the combination of a method of masking faults during margin testing of an electronic system, comprising: transmitting at least one of said one or more fault signals to a power control element in absence of margin testing. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 27, in combination with other limitations of the claims, none of the prior art of record teaches or suggests the combination of a method of masking faults during margin testing of an electronic system, comprising: generating an interrupt signal in response to a voltage associated with a power rail varying from a nominal value by more than a selected threshold. It is these limitations as they are claimed in the combination with other limitations of claim,

which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Response to Arguments

11. Applicant's arguments filed 07/19/2006 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach, "fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system and mask the at least one signal indicative of one or more faults by generating at least one signal indicative of absence of the one or more faults" as citied in claims 1, 22, 24, and 31.

Examiner position is that Coyle et al. teach fault bypass module (a failure capture module 2506) configured to indicate of one or more faults associated with one or more of said components (bus 2502) during margin testing of said electronic system (e.g. Fig.25, Col.34, lines 50-65, Col.35, lines 18-30, Col.36, lines 23-34) and mask the at least one signal indicative of one or more faults (not pass the value) by generating at least one signal indicative of absence of the one or more faults (pass the value) (e.g. Figs.28C, 28D, Col.39, line 42-Col.40, line 12).

-Applicant argues that the prior did not teach, "a fault bypass module incorporated in said computer server; said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components during margin testing of said computer server" as citied in claim 32.

Examiner position is that Coyle et al. teach a fault bypass module (a failure capture module 2506) incorporated in said computer server (bus 2502 of computer sever); said fault bypass module (failure capture module 2506) configured to mask signals indicative of one or more faults associated with one or more of said components (bus 2502) during margin testing of said computer server (e.g. Fig.25, Col.34, lines 62-65, Figs.28C, 28D, Col.39, line 42-Col.40, line 12).

Conclusion

12. Specifically Coyle et al. and Taraci et al. have been added to the other ground of rejection.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is 571 272 2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571 272 2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

August 29, 2006

BRYAN BUI
PRIMARY EXAMINER